**Amendments to the Claims:**

This listing of claims replaces all prior versions and listings of claims in the application.

**Listing of Claims:**

Claims 1 - 2 (Canceled)

Claim 3 (Previously Presented): A compound semiconductor field effect transistor as claimed in claim 10, wherein said $TiO_2$ layer has a stoichiometric composition.

Claim 4 (Previously Presented): A compound semiconductor field effect transistor as claimed in claim 10, wherein said $TiO_2$ layer has a non-stoichiometric composition.

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Claim 5 (Previously Presented): A compound semiconductor field effect transistor as claimed in claim 10, wherein said compound semiconductor device further includes first and second ohmic electrodes in contact with said compound semiconductor layer at both lateral sides of said gate electrode, and wherein $TiO_2$ layer is provided further at an interface between said first ohmic electrode and said compound semiconductor layer and between said second ohmic electrode and said compound semiconductor layer.

Claim 6 (Previously Presented): A compound semiconductor field effect transistor as claimed in claim 5, wherein said $TiO_2$ layer has a thickness allowing tunneling of carriers therethrough.

Claim 7 (Previously Presented): A compound semiconductor field effect transistor as claimed in claim 6 wherein said $TiO_2$ layer is provided so as to cover a surface of said compound semiconductor layer continuously from said first ohmic electrode to said gate electrode and from said gate electrode to said second ohmic electrode.

Claim 8 (Previously Presented): A semiconductor triode as claimed in claim 10, wherein said channel layer includes a two-dimensional electron gas.

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Claim 9 (Canceled)

Claim 10 (Currently Amended): A compound semiconductor field effect transistor, comprising:

a compound semiconductor layer including a channel layer and an electron supplying layer;

a gate electrode electrically contacting said compound semiconductor layer to control a current flow in said channel layer, said gate electrode having a multi-layer structure including a Ti layer, a Pt layer and an Au layer; and

an intermediate layer including a $TiO_2$ layer, formed between said Ti layer and said compound semiconductor layer,

wherein said intermediate layer ~~having~~ has a thickness of about 4nm.

Claim 11 (Previously Presented): The compound semiconductor field effect transistor as claimed in claim 10, wherein said compound semiconductor layer comprises an InGaAs layer

acting as said channel layer and an electron-supplying layer of InAlAs formed on said channel layer, and wherein said intermediate layer is formed between said Ti layer and said InAlAs layer.

Claim 12 (Previously Presented): The compound semiconductor transistor as claimed in claim 11, wherein said multi-layer structure comprises a layered structured in which a Pt layer and an Au layer are stacked on said Ti layer.

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Claim 13 (Previously Presented): The compound semiconductor field effect transistor as claimed in claim 10, wherein said $TiO_2$ layer is an insulating layer.

Claim 14 (Canceled)

Claim 15 (New): The compound semiconductor field effect transistor as claimed in claim 10, wherein said intermediate layer has a thickness of 4 nm.